What is claimed is:

1. A method of fabricating a semiconductor device, having one or more layers of materials deposited on a polysilicon layer, comprising the steps of:

forming one or more features on the semiconductor device, each of the one or more features having sidewalls;

selectively depositing a first spacer on the sidewalls of each of the one or more features; and

reoxidizing the semiconductor device.

2. The method of claim 1, wherein the step of forming one or more features comprises selectively etching the one or more features having sidewalls, thereby exposing the one or more layers of materials.

3. The method of claim 2, wherein the polysilicon layer serves as an etch stop.

4. The method of claim 1, wherein the step of selectively depositing a first spacer further comprises limiting deposition time to be less than incubation time.

5. The method of claim 1, wherein the step of selectively depositing a first spacer comprises selectively depositing a thin silicon nitride.

6. A method of fabricating a semiconductor device, having one or more layers of materials deposited on a polysilicon layer, comprising the steps of:

selectively etching the semiconductor device to form one or more features having sidewalls exposing the one or more layers of materials, wherein the polysilicon layer serves as an etch stop;

selectively depositing a first spacer on the sidewalls of each of the one or more features; and

reoxidizing the semiconductor device.

7. The method of claim 6, wherein the step of selectively depositing a first spacer further comprises limiting deposition time to be less than incubation time.

8. The method of claim 6, wherein the step of selectively depositing a first spacer comprises selectively depositing a thin silicon nitride.

9. A method of forming a structure for controlling current flow between a source and a drain region in a semiconductor device, comprising the steps of:

forming an insulating layer on a semiconductor wafer;

forming a conductive layer over the insulating layer;

forming a gate by etching, using the insulating layer as an etch stop, wherein the gate has sidewalls exposing the conductive layer and some portion of the insulating layer;

selectively forming a first oxidation barrier on the sidewalls of the gate; and

reoxidizing the structure.

10. The method of claim 9, wherein the step of selectively forming a first oxidation barrier comprises selectively depositing a thin silicon nitride on the gate without depositing any on the source and the drain regions.

11. A method of forming a structure for controlling current flow between a source and a drain region in a semiconductor device, wherein the semiconductor device is composed of a semiconductor wafer, an insulating layer disposed over the semiconductor layer, and a conductive layer disposed over the insulating layer, the method comprising the steps of:

forming a gate having sidewalls exposing the conductive layer and some portion of the insulating layer;

depositing a thin silicon nitride on the gate;

avoiding depositing the thin silicon nitride on the source and the drain region;

forming a first oxidation barrier on the sidewalls of the gate; and

reoxidizing the structure.

12. The method of claim 11, wherein the step of avoiding depositing the thin silicon nitride on the source and the drain regions comprises limiting deposition time to be less than incubation time.

13. A semiconductor device, comprising:

a layer of polysilicon;

one or more active areas;

one or more features protruding from the polysilicon and having sidewalls, the one or more features separating the one or more active areas, each of the one or more features including:

a portion of the polysilicon layer,

one or more layers of conductive materials deposited on the layer of polysilicon, and

a spacer selectively deposited on the sidewalls of the one or more features; and

a layer of silicon oxide deposited on the semiconductor device, wherein the spacer is interposed between the layer of silicon dioxide and the sidewalls.

14. The semiconductor device of claim 13, wherein the selective spacer comprises silicon nitride.

15. The semiconductor device of claim 13, wherein the one or more layers of conductive materials comprise tungsten silicide.

16. A semiconductor device, comprising:

a layer of polysilicon;

one or more active areas; and

one or more features protruding from the polysilicon and having sidewalls, the one or more features separating the one or more active areas, each of the one or more features comprising:

one or more layers of conductive materials deposited on the layer of polysilicon, at least one layer of which includes tungsten silicide; and

a silicon nitride spacer selectively deposited on the sidewalls of the one or more features; and

a layer of silicon oxide deposited on the semiconductor device, wherein the silicon nitride spacer is interposed between the layer of silicon oxide and the sidewalls of the one or more features.

17. A gate electrode, comprising:

one or more layers of conductive materials etched to form features having sidewalls exposing the one or more layers;

a selectively deposited spacer, wherein the spacer is deposited only on the feature sidewalls;

a layer of silicon oxide disposed over the gate electrode surface.

18. The gate electrode of claim 17, wherein the one or more layers of conductive materials comprise tungsten silicide.

19. The gate electrode of claim 17, wherein the selectively deposited spacer comprises silicon nitride.

20. A semiconductor device having a device having an electrode and an active area, wherein the electrode has a side and the active area has a surface, comprising:

a spacer, wherein

the spacer covers the electrode; and

the spacer provides unobstructed physical communication with the active area.

21. The semiconductor device of claim 20, wherein:

the spacer covers the side of the electrode; and

the spacer provides unobstructed physical communication with the surface of the active area.

22. A spacer for a semiconductor device, wherein:

the spacer is disposed to substantially prevent physical communication between a first layer of the semiconductor device and a first area of the semiconductor device; and

the spacer is disposed to provide unobstructed physical communication between the first layer of the semiconductor device and a second area of the semiconductor device.

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